Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2017

Subject Name: Embedded System Design

Subject Code: 5TE01EMD1 **Branch: M.Tech(VESD)**

Semester: 1 **Date: 24/03/2017** **Time: 10:30 To 01:30** **Marks: 70**

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

SECTION – I

Q-1		**Attempt the Following questions**	**(07)**
	a.	Define the term system.	**1**
	b.	Define the term an embedded system.	**1**
	c.	State the constraints consider when an embedded system is designed.	**1**
	d.	State any five examples of embedded systems.	**1**
	e.	State the different interrupt sources in embedded processors or controllers.	**1**
	f.	Define the term RTOS.	**1**
	g.	Define the term development kit.	**1**
Q-2		**Attempt all questions**	**(14)**
	a)	Explain in detail different interrupt handling mechanism.	**6**
	b)	Classify the embedded systems and explain each of them in detail.	**4**
	c)	Explain in brief any four concepts used during design process in embedded system.	**4**
		OR	
Q-2		**Attempt all questions**	**(14)**
	a)	Explain in detail source engineering tool.	**6**
	b)	Explain in detail skills required for an embedded system designer	**4**
	c)	Draw the diagram of the components of embedded system hardware. Explain in brief main three components embedded into embedded system.	**4**
Q-3		**Attempt all questions**	**(14)**
	a)	Write short notes on “embedded processors in a system”.	**7**
	b)	What is the full form of IDE? Explain its features.	**7**
		OR	
Q-3	**a)**	Explain in detail different challenges in embedded system design.	**7**
	b)	Explain in detail with diagrams device programmer	**7**

SECTION – II

Q-4		**Attempt the Following questions**	**(07)**
	a.	Explain in brief big-endian data representation.	**1**
	b.	Explain in brief little-endian data representation.	**1**
	c.	Explain in brief Harvard architecture.	**1**
	d.	Explain in brief von Neumann architecture.	**1**
	e.	What data types does the C55x support?	**1**
	f.	How many accumulators does the C55x have?	**1**
	g.	How many types of interrupts support by ARM? State their names.	**1**
Q-5		**Attempt all questions**	**(14)**
	a)	Explain in detail with examples different addressing modes of ARM 7 processor.	**7**
	b)	Write short notes on " caches as memory system mechanisms"	**7**
		OR	**(14)**
Q-5	**a)**	Explain in brief supervisor mode, exceptions and traps w.r.to. ARM7 processor.	**7**
	b)	Write short notes on " MMUs as memory system mechanisms"	**7**
Q-6		**Attempt all questions**	**(14)**
	a)	State the steps perform by ARM7 and C55X when responding to an interrupt.	**7**
	b)	Explain in detail data flow graphs.	**7**
		OR	
Q-6		**Attempt all Questions**	**(14)**
	a)	Explain in detail CPU performance.	**7**
	b)	Explain in detail control/data flow graphs.	**7**